APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,051	11/25/2003	Ernest P. Chen	042390.17529	7780

			EXAMINER
8791	7590	08/22/2006	GEIB, BENJAMIN P

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ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/723,051	CHEN, ERNEST P.
	Examiner	Art Unit	
	Benjamin P. Geib	2181	.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 May 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>57-72</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>57-72</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/18/2006

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 57-72 have been examined.

2.   It is hereby acknowledged that the following papers have been received and

placed of record in the file: Amendment as received on 05/25/2006.

Withdrawn Rejections

3.   Applicant, via amendment, has overcome the 35 U.S.C. § 101 rejections set forth

in the previous Office Action.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 57, 58, 60-63, 65-67, and 69-72 are rejected under 35 U.S.C. 102(b) as

being anticipated by Turley, "Advanced 80386 Programming Techniques" (Herein

referred to as Turley).

6.   Referring to claim 57, Turley has taught a method comprising:

setting a first indicator *[exchanging an instruction byte with the breakpoint*

opcode 0xCC; See 2nd and 3rd paragraphs on page 326], the first indicator comprising

only a portion of a computer program instruction *[The breakpoint opcode is a single*

byte, while instructions can be multiple bytes. Therefore, the indicator comprises only a

portion of the a multiple byte instruction; See 3ʳᵈ paragraph on page 326]; and

halting execution of the computer program instruction in response to setting the

first indicator *[See 3ʳᵈ and 4ᵗʰ paragraphs on page 326].*

7.   Referring to claim 58, <u>Turley</u> has taught the method of claim 57, wherein the first

indicator comprises one of only a portion of a computer program opcode or only a

portion of a computer program micro-operation *[The breakpoint opcode comprises a*

portion (a byte) of a multiple byte instruction (i.e. micro-operation); See 3ʳᵈ paragraph on

page 326].

8.   Referring to claim 60, <u>Turley</u> has taught the method of claim 57, further

comprising:

setting a second indicator *[exchanging the breakpoint opcode with the first byte*

of the original instruction; See 1ˢᵗ full paragraph on page 327]; and

finishing execution of the computer program instruction in response to setting the

second indicator *[See 1ˢᵗ full paragraph on page 327].*

9.   Referring to claim 61, <u>Turley</u> has taught the method of claim 60, wherein the

second indicator comprises a data bit held in a register *[The first byte of the original*

instruction is 8 bits and held in a memory location, which is a register; See 3ʳᵈ

paragraph on page 326 and 3ʳᵈ paragraph on page 327].

10.   Referring to claim 62, <u>Turley</u> has taught an apparatus comprising:

a processor *[80386 microprocessor; See page 326]; and*

a first indicator *[breakpoint opcode 0xCC; See 2nd and 3rd paragraphs on page 326]* configurable to halt execution of a computer program instruction by the processor, wherein the first indicator comprises only a portion of the computer program instruction *[The breakpoint opcode is a single byte, while instructions can be multiple bytes. Therefore, the indicator comprises only a portion of the a multiple byte instruction; See 3rd paragraph on page 326]*.

11.   Referring to claim 63, <u>Turley</u> has taught the apparatus of claim 62, wherein the first indicator comprises one of only a portion of a computer program opcode or only a portion of a computer program micro-operation *[The breakpoint opcode comprises a portion (a byte) of a multiple byte instruction (i.e. micro-operation); See 3rd paragraph on page 326]*.

12.   Referring to claim 65, <u>Turley</u> has taught the apparatus of claim 62, further comprising:

a second indicator *[the first byte of the original instruction]* configurable to instruct the processor to finish execution of the computer program instruction *[See 1st full paragraph on page 327]*.

13.   Referring to claim 66, <u>Turley</u> has taught the apparatus of claim 65, wherein the second indicator comprises a data bit held in a register coupled to the processor *[The first byte of the original instruction is 8 bits and held in a memory location, which is a register, coupled to the processor; See 3rd paragraph on page 326 and 3rd paragraph on page 327]*.

14.   Referring to claim 67, <u>Turley</u> has taught a system comprising:

a processor *[80386 microprocessor]* to execute a computer program instruction *[See page 326]*;

a memory coupled to the processor, the memory to store the computer program instruction to be executed by the processor *[The code (i.e. computer program instruction) is inherently stored in a memory coupled to the processor since a memory is needed to write to; See 3rd paragraph on page 327]*; and

an indicator *[breakpoint opcode 0xCC; See 2nd and 3rd paragraphs on page 326]* configurable to control execution of the computer program instruction by the processor, wherein the indicator comprises only a portion of the computer program instruction *[The breakpoint opcode is a single byte, while instructions can be multiple bytes. Therefore, the indicator comprises only a portion of the a multiple byte instruction; See 3rd paragraph on page 326]*.

15.   Referring to claim 69, <u>Turley</u> has taught the system of claim 67, wherein the indicator comprises one of only a portion of a computer program opcode or only a portion of a computer program micro-operation *[The breakpoint opcode comprises a portion (a byte) of a multiple byte instruction (i.e. micro-operation); See 3rd paragraph on page 326]*.

16.   Referring to claim 70, <u>Turley</u> has taught the system of claim 67, wherein the indicator comprises a data bit of a computer program opcode *[The breakpoint opcode is 8 bits and, therefore, comprises a data bit of a computer program opcode; See 3rd paragraph on page 326]*.

17.   Referring to claim 71, <u>Turley</u> has taught the system of claim 67, further

comprising:

another indicator *[the first byte of the original instruction]* configurable to instruct

the processor to finish execution of the computer program instruction *[See 1st full*

paragraph on page 327].

18.   Referring to claim 72, <u>Turley</u> has taught the system of claim 71, wherein the

another indicator comprises a data bit held in a register coupled to the processor *[The*

first byte of the original instruction is 8 bits and held in a memory location, which is a

register, coupled to the processor; See 3rd paragraph on page 326 and 3rd paragraph on

page 327].

Claim Rejections - 35 USC § 103

19.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

20.   Claims 59 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable

over <u>Turley</u> in view of <u>Deao</u> et al., U.S. Patent No. 6,016,555 (Herein referred to as

<u>Deao</u>).

21.   Referring to claim 59, <u>Turley</u> has taught the method of claim 57, wherein the first

indicator is a byte of a computer program opcode *[See 2nd paragraph on page 326]*.

Turley does not disclose expressly that the indicator is only one data bit.

Deao discloses a software breakpoint (i.e. indicator) that is only one data bit of a

computer program opcode [Deao; column 5, lines 10-15].

At the time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the indicator of Turley to be only one data bit of a

computer program opcode as taught by Deao.

The suggestion/motivation for doing so would have been that the debug software

only needs to replace a single bit and, further, that the original opcode is decoded and

passed to the execution unit [Deao; column 5, lines 15-19].

22.   Referring to claim 64, given the similarities between claim 59 and claim 64 the

arguments as stated for the rejection of claim 59 also apply to claim 64.

23.   Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Turley.

24.   Referring to claim 68, Turley has taught the system of claim 67.

Turley does not disclose expressly that the memory comprises Dynamic Random

Access Memory (DRAM).

However, Examiner takes Official Notice that using Dynamic Random Access

Memory (DRAM) for memory is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the memory of Turley to be DRAM since doing so would

allow a large amount of data to be stored in a small area.

Response to Arguments

25.   Applicants arguments filed on May 25, 2006, have been fully considered but they

are not found persuasive.

26.   Applicant argues the novelty/rejection of claim 57 on pages 5-6 of the remarks, in

substance that:

> "Applicants asserts that Turley fails to disclose an indicator comprising only a portion of a
> computer program instruction" (2nd full paragraph on page 6)

These arguments are not found persuasive for the following reasons:

The breakpoint opcode of Turley is a single byte and is used to replace the first

byte of a multiple byte instruction (See 3rd paragraph on page 326). Therefore, Turley

has taught an indicator (i.e. breakpoint opcode) that comprises only a portion of a

computer program instruction (a multiple byte instruction).

Conclusion

27.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28.   The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

29.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Buser, U.S. Patent Application Publication No. 2004/0030870, teaches a CPU halt identifier field that comprises a portion of an instruction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

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8/18/2006